REMARKS

The examiner relies on the video data buffer 202 of Haskell et al to meet the requirement in claim 1 for a smoothing buffer.

Applicant has asserted that the video data buffer 202 of Haskell et al is the 1.8 megabyte decoder buffer that is assumed by the MPEG Standard to be present in an MPEG compliant decoder and that the decoder buffer receives a picture at a constant bit rate and holds the picture until its decode time stamp, whereupon the picture is instantaneously removed from the buffer and supplied to the decoder 204 for decoding. In a conventional configuration, the video display control 203 would extract the data from the video data buffer 202 when the STC value increases to the value of the oldest DTS of the video data.

The examiner asserts that the disclosure of Haskell et al at column 1, lines 19-23 suggests that the data channel that supplies data to the buffer 202 might be a variable bit rate channel. The paragraph starting at column 2, line 51 of Haskell et al shows that the ATM data channel between the multiplexer unit 100 and demultiplexer unit 200 conveys a plurality of channels of video and corresponding audio. Thus, the data rate of the channel that actually feeds the video data buffer 202 will generally be less than the data rate of the ATM data channel that feeds the demultiplexer unit 200, and whether the ATM data channel is variable bit rate or constant bit rate tells us nothing about the data rate of the channel that feeds the video data from the systems decoder and SCR extractor 201 to the video data buffer 202. In addition, although the bit rate of the ATM data channel might not be constant, Haskell et al emphasizes at column 3, lines 49-53, that the channel data rate is constant for an interval that can be a long as 700 ms. Thus, the channel data rate is in fact constant over as many as 21 frames.

The examiner asserts that the explanation at column 5, lines 46-63 of Haskell et al relates to loading of the data into the video data buffer 202. Applicant respectfully disagrees. The paragraph in question relates to use of the jitter delay D_j to alleviate underflow. Referring to column 5, lines 11-14, the video display control 203 "waits until the STC-D_j value increases to the value of the oldest DTS [of the video data]. It then extracts the coded video data for the corresponding image representation from video data buffer 202..." By

reducing the value that is compared with the oldest DTS from STC to STC-D_j, the video display control 203 does not adjust the time at which loading of data into the data buffer commences but on the contrary delays extraction of the coded video data from the buffer 202. Accordingly, during this delay time D_j additional video data can accumulate in the video data buffer 202 and the possibility of underflow, i.e. finding that the access unit that is currently being extracted from the video data buffer has not yet been fully loaded into the video data buffer, is avoided. The video display control 203 does not exert any control over loading of data into the video data buffer, and, in particular, the jitter delay value D_j does not influence the time at which video data corresponding to an image representation is loaded into the buffer.

The examiner observes that Haskell et al points out that the addition of the jitter delay D_j causes "an extra accumulation of data in the buffer prior to decoding" and asserts that this implies that the load commences at a specified time prior to DTS. This is not the case. In Haskell et al, the extra accumulation of data occurs because the jitter delay D_j postpones the time at which the data is removed from the buffer.

Respectfully submitted,

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